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### 1 [Low Energy Data Management for Different On-Chip Memory Levels in Multi-Context Reconfigurable Architectures](#)

M. Sanchez-Elez, M. Fernandez, M. Anido, H. Du, N. Bagherzadeh, R. Hermida

March 2003 DATE '03: Proceedings of the conference on Design, Automation and Test in Europe - Volume 1, Volume 1

Publisher: IEEE Computer Society

 Full text available: [Publisher Site](#), [Pdf \(141.12 KB\)](#) **Additional Information:** [full citation](#), [abstract](#), [references](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 11, Citation Count: 1

This paper presents a new technique to improve the efficiency of data scheduling for multi-context reconfigurable architectures targeting multimedia and DSP applications. The main goal is to improve application energy consumption. Two levels of on-chip ...

### 2 [Spatial join techniques](#)

Edwin H. Jacox, Hanan Samet

March 2007 ACM Transactions on Database Systems (TODS), Volume 32 Issue 1

Publisher: ACM

 Full text available: [Pdf \(1.24 MB\)](#)
**Additional Information:** [full citation](#), [appendices and supplements](#), [abstract](#), [references](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 50, Downloads (12 Months): 367, Citation Count: 2

A variety of techniques for performing a spatial join are reviewed. Instead of just summarizing the literature and presenting each technique in its entirety, distinct components of the different techniques are described and each is decomposed into an ...

Keywords: External memory algorithms, plane-sweep, spatial join

### 3 [GPUTeraSort: high performance graphics co-processor sorting for large database management](#)

Naga Govindaraju, Jim Gray, Ritesh Kumar, Dinesh Manocha

June 2006 SIGMOD '06: Proceedings of the 2006 ACM SIGMOD international conference on Management of data

Publisher: ACM

 Full text available: [Pdf \(1.46 MB\)](#)
**Additional Information:** [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 18, Downloads (12 Months): 170, Citation Count: 15

We present a novel external sorting algorithm using graphics processors (GPUs) on large databases composed of billions of records and wide keys. Our algorithm uses the data parallelism within a GPU along with task parallelism by scheduling some of the ...

#### 4 [A data scheduler for multi-context reconfigurable architectures](#)



Marcos Sanchez-Elez, Milagros Fernández, Roman Hermida, Rafael Maestre, Fadi Kurdahi, Nader Bagherzadeh

September 2001 ISSS '01: Proceedings of the 14th international symposium on Systems synthesis  
Publisher: ACM

Full text available: Pdf (228.09 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 14, Citation Count: 0

In this paper, we present an approach to the problem of data scheduling for multi-context reconfigurable architectures targeting DSP applications. The main goal is to improve application execution time, through the integration of the data scheduler ...

#### 5 [Realtime ray tracing of dynamic scenes on an FPGA chip](#)



Jörg Schmittler, Sven Woop, Daniel Wagner, Wolfgang J. Paul, Philipp Slusallek

August 2004 HWS '04: Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware  
Publisher: ACM

Full text available: Pdf (1.72 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 97, Citation Count: 9

Realtime ray tracing has recently established itself as a possible alternative to the current rasterization approach for interactive 3D graphics. However, the performance of existing software implementations is still severely limited by today's CPUs, ...

#### 6 [A Complete Data Scheduler for Multi-Context Reconfigurable Architectures](#)

M. Sánchez-Élez, M. Fernández, R. Maestre, F. Kurdahi, R. Hermida, N. Bagherzadeh

March 2002 DATE '02: Proceedings of the conference on Design, automation and test in Europe  
Publisher: IEEE Computer Society

Full text available: Pdf (127.63 KB) Additional Information: [full citation](#), [abstract](#), [cited by](#)

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 13, Citation Count: 3

A new technique is presented in this paper to improve the efficiency of data scheduling for multi-context reconfigurable architectures targeting multimedia and DSP applications. The main goal is to improve the application execution time minimizing external ...


#### 7 [Efficient mapping of hierarchical trees on coarse-grain reconfigurable architectures](#)



F. Rivera, M. Sanchez-Elez, M. Fernandez, R. Hermida, N. Bagherzadeh

September 2004 CODES+ISSS '04: Proceedings of the 2nd IEEE/ACM/FIP international conference on Hardware/software codesign and system synthesis  
Publisher: ACM

Full text available: Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

 Pdf (316.12 KB)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 17, Citation Count: 0

Reconfigurable architectures have become increasingly important in recent years. In this paper we present an approach to the problem of executing 3D graphics interactive applications onto these architectures. The hierarchical trees are usually implemented ...

Keyw ords: SIMD, computer graphics, hierarchical trees, multimedia, reconfigurable architecture


## 8 Hardware acceleration of graphics and imaging algorithms using FPGAs



Pavel Zemcik

April 2002. SCCG '02: Proceedings of the 18th spring conference on Computer graphics

Publisher: ACM

Full text available:  Pdf (842.76 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 100, Citation Count: 1

Computer graphics algorithms and algorithms used in image processing are generally computationally expensive. This fact is the reason why people struggle to accelerate such algorithms using any reasonable means. The traditional sources of speedup are ...

Keyw ords: FPGA, computer graphics, hardware acceleration, image processing

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